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EXAMINER	
NEURAUTER, GEORGE C	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL R. KRAUSE, ALAN F. BENNER,
DAVID J. GARCIA, and RENATO J. RECIO

Appeal 2008-1940
Application 09/980,920[1]
Technology Center 2100

Decided: November 17, 2008

Before JAMES D. THOMAS, JEAN R. HOMERE, and THU A. DANG, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1 through 34. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

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[1] Filed on April 11, 2002. The real party in interest is Hewlett Packard Development Co, L.P.

Appellants' Invention

Appellants invented a method and system for managing memory in a distributed computing environment. (Spec. 1.) As depicted in Figure 18, a first host processor (702) binds a remote key (746) to a contiguous memory address (744) in the first host processor, and sends the bound remote key including the memory address to a second host processor (704) on a communication fabric (722) via their respective network interface controls (NIC 714, 734). The second host processor (704) subsequently sends the remote key to the first host processor on the communication fabric (722) via the NICs in order to access the contiguous memory address designated by the remote key. (*Id.* 35-37.)

Illustrative Claim

Independent claim 1 further illustrates the invention. It reads as follows:

1. A method of managing memory in a distributed computer system, the method comprising:

binding a remote key to a first address presenting a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode including a first processor and the first memory;

sending the bound remote key and first address from the first host processor endnode to a second host processor endnode on a communication fabric via a first networking interface controller (NIC) in the first host

processor endnode and a second NIC in the second host processor endnode, wherein the second host processor endnode includes a second processor and a second memory; and

performing a remote direct memory access operation from the second host processor endnode with a second consumer process stored in the second memory to access the contiguous memory address range including sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Futral	US 5,991,797	Nov. 23, 1999
Forin	US 6,360,220 B1	Mar. 19, 2002
Regnier	US 6,647,423 B2	Nov. 11, 2003

Rejections on Appeal

The Examiner rejects the claims on appeal as follows:

1. Claims 1, 2, 6, 7, 9 through 13, 16, 17, 19, 20, 23 through 29, 32, and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Futral.

2. Claims 3 through 5, 8, 21, 22, and 25 stand rejected under 35 U.S.C. § 103(a) as being anticipated by Futral and Regnier.

3. Claims 14, 15, 18, 30, 31, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Futral and Forin.

Appellants' Contentions

Appellants argue that Futral does not teach a second host processor that performs an RDMA operation to access the contiguous memory address, as designated by the bound remote key, in the first host processor on a communication fabric via a first NIC and a second NIC, as recited in independent claim 1. (App. Br. 8-10, Reply Br. 3-5.) Particularly, Appellants argue that Futral discloses an I/O device that transfers data between a requesting host processor and an I/O unit. However, Appellants argue that neither the I/O device nor the I/O unit is equivalent to the second host processor, as claimed. Therefore, Appellants submit that Futral does not teach a second host processor that performs the RDMA operation, as required by claim 1. (*Id.*)

Examiner's Findings

In response, the Examiner finds that Futral's disclosure of using an RDMA object created by an I/O device to directly transfer data between generic units such as a host processor and an I/O unit on a SAN fabric via a

first NIC and a second NIC teaches the claimed limitations. (Ans. 15-20.) Consequently, the Examiner finds that Futral anticipates independent claim 1. (*Id.*)

II. ISSUE

Thus, the pivotal issue before us is whether Appellants have shown that the Examiner erred in finding that Futral anticipates the claimed invention. Particularly, the issue turns on whether Futral's disclosure of using an I/O device to transfer data between a requesting host processor and an I/O unit teaches a second host processor that performs an RDMA operation to access data in the memory address in a first host processor, as recited in independent claim 1.

III. FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Futral

1. A depicted in Figure 2, Futral discloses an I/O device (50) that is used to directly transfer data between an application program's buffer on a host computer and an I/O unit (52) coupled to the I/O device (50). (Col. 2, ll. 50-55.)

2. Futral discloses that the I/O unit (52) is an autonomous device that includes its own physical memory, one or more processors, one or more I/O processors and other I/O resources. (Col. 3, ll. 50-53.)

3. Futral discloses that host systems and I/O units are generic devices. They can be implemented as servers, PCs, and other workstations. (Col. 6, ll. 37-47.)

4. The I/O device (50) creates a remote direct memory access (RDMA) object that identifies memory registered by a process that a remote transport agent can access. RDMA allows the I/O device to directly transport data between the requesting host buffer and the I/O unit. (Col. 7, ll. 5-17.)

5. The I/O device transmits an RDMA object to the requesting host processor to indicate the address location in the I/O unit where the requested data resides. The requesting host processor subsequently uses the RDMA to access the designated address location in the I/O unit on the SAN fabric via the NIC of the requesting host and the NIC of the I/O unit. (Col. 7, ll. 18-34.)

IV. PRINCIPLES OF LAW

ANTICIPATION

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005), citing *Minn.*

Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565 (Fed. Cir. 1992). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

V. ANALYSIS

35 U.S.C. § 102

As set forth in the Findings of Fact section, Futral discloses an I/O unit having a memory and one or more processors. (FF. 2.) We note that the disclosed I/O unit, similarly to the claimed second host processor, includes a memory and a processor. Therefore, the disclosed I/O unit reasonably teaches the claimed second host processor. Further, Futral discloses an I/O device that creates an RDMA object for transferring data between the buffer of a requesting host processor and the I/O unit on a SAN fabric via the NIC of the requesting processor and the NIC of the I/O unit. (FF. 1, 3-4.) Particularly, the I/O device informs the requesting host processor of an address location in the I/O unit designated by the RDMA object. The requesting host processor subsequently uses the RDMA object to access the designated address location in the I/O unit on the SAN fabric via

the NIC of the requesting host processor and the I/O unit. (FF. 5.) We find that Futral's I/O device coupled with the I/O unit (I/O device-unit) reasonably teaches the claimed first host processor. In other words, similarly to the claimed first host processor, the resulting I/O device-unit sends a created RDMA object to a requesting second host to specify the memory address in the I/O device-unit where the requested data is stored. Further, similarly to the claimed second host processor, the requesting host uses the RDMA object to access the specified memory location in the resulting I/O device-unit where the data is located. It follows that Appellants have not shown that the Examiner erred in finding that Futral anticipates claim 1.

Appellants did not provide separate arguments with respect to the rejection of claims 1, 2, 6, 7, 9 through 13, 16, 17, 19, 20, 23 through 29, 32, and 33. Therefore, we select independent claim 1 as being representative of the cited claims. Consequently, claims 2, 6, 7, 9 through 13, 16, 17, 19, 20, 23 through 29, 32, and 33 fall together with representative claim 1. 37 C.F.R. § 41.37(c)(1)(vii).

35 U.S.C. § 103

Appellants argue that dependent claims 3 through 5, 8, 14, 15, 18, 21, 22, 25, 30, 31, and 34 recite the limitations of independent claims 1 or independent claim 19, and that neither Regnier nor Forin remedies the deficiencies of Futral, as argued above. (App. Br. 11, Reply Br. 5.)

Therefore, Appellants submit that Futral taken in combination with either Regnier or Forin does not render the cited claims unpatentable. (*Id.*) As discussed above, we have found no such deficiencies in the Futral reference for either Regnier or Forin to cure. It follows that Appellants have not shown that the Examiner erred in concluding that the combination of Futral and Regnier renders claims 3 through 5, 8, 21, 22, and 25 unpatentable. Similarly, Appellants have not shown that the Examiner erred in concluding that the combination of Futral and Forin renders claims 14, 15, 18, 30, 31, and 34 unpatentable.

VI. CONCLUSIONS OF LAW

1. Appellants have not shown that the Examiner erred in finding that Futral anticipates claims 1, 2, 6, 7, 9 through 13, 16, 17, 19, 20, 23 through 29, 32, and 33 under 35 U.S.C. § 102(e).

2. Appellants have not shown that the Examiner erred in concluding that the combination of Futral and Regnier renders claims 3 through 5, 8, 21, 22, and 25 unpatentable under 35 U.S.C. § 103(a).

3. Appellants have not shown that the Examiner erred in concluding that the combination of Futral and Forin renders claims 14, 15, 18, 30, 31, and 34 unpatentable under 35 U.S.C. § 103(a).

VII. DECISION

We affirm the Examiner's decision rejecting claims 1 through 34.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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